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EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,544	BUSABA ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 have been examined.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: all those on pages 2 and 6-8, i.e. no reference signs are included in the drawings. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because they label the figures twice, once with a general label, and once with a label containing a description. Furthermore, the drawings appear to have been previously published. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

6. The spacing of the lines of the specification is such as to make reading and entry of amendments difficult. New application papers with lines double spaced on good quality paper are required. Specifically, see pages 12 and 15 for improper spacing of the claims.

7. The disclosure is objected to because of the following informalities:

a. Pages 2 and 6-8 of the specification contain reference numbers that attempt to refer to the drawings. However, the drawings do not contain the reference numbers recited, or any reference numbers for that matter. Please amend the specification to remove or correct these references, and/or correct the drawings to provide the reference numbers.

b. Page 3 of the specification states that the control pipeline has four stages on lines 13-16. However, page 4 states that the control pipeline has three stages on lines 21-23. It is unclear which is the correct amount of stages for the control pipeline. Please correct this language to more particularly define the invention.

Appropriate correction is required.

Claim Objections

8. Claims 1 and 11 is objected to because of the following informalities:

a. Regarding claim 1, please change the claim language "1 Claim 1" to simply read "1."

b. Regarding claim 11, please change the claim language "mask generate process" to read "mask generation process" in order to be more grammatically correct.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-3, 5-6, 9-10, and 13-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 1 recites the limitation "the operands" in its tenth line. There is insufficient antecedent basis for this limitation in the claim. Please amend the claim language to correct this antecedent basis problem.

12. Claim 1 recites the limitation "an integer execution unit (FXU) having an Instruction Decode and Dispatch Unit (I-Unit) and an integer execution unit (E-unit) of a central processor (CP). It is unclear how the integer execution unit can contain another integer execution unit. Furthermore, one of ordinary skill in the art would have recognized that the acronyms beginning with the letter "F", such as "FXU", are generally reserved for those operations taking place on floating-point numbers rather than integer numbers. Please correct the claim language to more distinctly point out the structure of the processor as claimed.

13. Claim 2 recites the limitation "the process" in its first line. There is insufficient antecedent basis for this limitation in the claim. Please amend the claim language to correct this antecedent basis problem. Furthermore, it is unclear whether "the process" refers to the method of the parent claim 1, or if it refers to the partial instruction which is executing, or something else

completely. For the purposes of this examination, the Examiner will assume that "the process" refers to the method as claimed in the parent claim 1.

14. Claim 3 recites the limitation "the result" in its fifth line. There is insufficient antecedent basis for this limitation in the claim. Please amend the claim language to correct this antecedent basis problem. Furthermore, it is unclear whether "the result" refers to a result of the instruction executing, the output of the ALU, the result of the method of its parent claim, or something else completely. For the purposes of this examination, the Examiner will assume that "the result" refers to the result of the calculations performed within the ALU.

15. Claim 3 recites the limitation "the input operands" in its fourth line. There is insufficient antecedent basis for this limitation in the claim. Please amend the claim language to correct this antecedent basis problem.

16. Claim 5 recites the limitation "the controls to the computer system ALU" in its fourth line. There is insufficient antecedent basis for this limitation in the claim. Please amend the claim language to correct this antecedent basis problem.

17. Claim 5 recites the limitation "...the second partitioned process is used for reading and loading operands into a plurality of FXU input register of said computer system's FXU which cycle determines whether the timing critical function of said predetermined cycle is valid for an instruction to be executed." This language is not grammatically correct English, and it is unclear what "which cycle determines" means. Generally, language such as "which cycle determines" implies that there would have been a cycle stated which determined the outcome of something. However, no such cycle is stated. Please correct the claim language to more clearly define the invention as claimed.

18. Claim 6 recites the limitation "wherein said third cycle is a dispatch cycle." However, claim 5, which is the parent claim of claim 6, recites the limitation "wherein during the third cycle the contents of the result register are sent to an architected General Purpose Register file," which implies that the third cycle in the context of claim 5 is a register write cycle such as stage s9 of the NPC pipeline of Leung (see Col. 12 lines 18-31), not a dispatch cycle as claimed in claim 6. Furthermore, claim 4, the parent claim of claim 5, claims both a dispatch cycle and a third cycle separately, implying that they are, in fact, different stages. Because a dispatch stage clearly performs a different operation than does a register write stage, it is unclear how a stage that performs a register write function can also be a dispatch cycle. Please correct the claim language to clarify this situation. For the purposes of this examination, it will be assumed that the dispatch cycle was meant to be claimed as the dispatch cycle in claim 4.

19. Claim 9 recites the limitation "second partitioned process said pipeline stages" in its fourth and fifth lines. There is insufficient antecedent basis for this limitation in the claim. Please amend the claim language to correct this antecedent basis problem. Furthermore, it is unclear whether "second partitioned process said pipeline stages" refers to the pipeline stages of the partitioned process, stages of the other partitioned process, or something else completely. For the purposes of this examination, the Examiner will assume that "second partitioned process said pipeline stages" refers to the three cycles of the second partitioned process as recited in claim 4.

20. Claim 10 recites the limitation "I-unit instruction pipeline" in its second line. There is insufficient antecedent basis for this limitation in the claim. Please amend the claim language to correct this antecedent basis problem.

21. Claim 13 recites the limitation "the execution (e0) stage" on its third line, as well as the limitation "the E0 cycle" on its last line. There is insufficient antecedent basis for these limitations in the claim. Please amend the claim language to correct this antecedent basis problem. Furthermore, it is unclear which pipeline these stages refer to, if any, if they are the same pipeline, and whether the e0 stage and the E0 cycle are the result of a grammatical error, refer to different limitations, or if they actually refer to the same limitation.

22. Claim 14 recites the limitations "the mask generator logic" and "the I-unit instruction unit" in lines 2-4. There is insufficient antecedent basis for these limitations in the claim. Please amend the claim language to correct these antecedent basis problems.

23. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite in that it fails to point out what is included or excluded by the claim language by its use of "implied". This claim is an omnibus type claim. Please correct the claim language to more clearly define what the invention is claimed to be.

24. Claim 16 recites the limitation "the execution stages" on its third line. There is insufficient antecedent basis for this limitation in the claim. Please amend the claim language to correct this antecedent basis problem. Furthermore, it is unclear whether "the execution stages" refer to stages of a pipeline, and if so what pipeline, or if it refers to something else completely. For the purposes of this examination, the Examiner will assume that "the execution stages" refer to execution stages of the pipeline that contains the predetermined cycle pipeline stage.

Claim Rejections - 35 USC § 102

25. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

26. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Leung et al., U.S. Patent No. 5,948.098.

27. Regarding claim 1, Leung has taught a method for use in a computer system having an integer execution unit (FXU) (232 of Fig.4) having an Instruction Decode and Dispatch Unit (I-Unit) (242 of Fig.4) and an integer execution unit (E-Unit) (234 of Fig.4) of a central processor (CP) (202 of Fig.3) of the computer system which contains an arithmetic and logical unit (ALU) (230 of Fig.9 and 263 of Fig.5) which is capable of performing arithmetic functions including binary addition, subtraction, and logical operations such as logical and, logical or, and logical exclusive or (see Col.11 lines 53-61), wherein said logical operations are bit maskable to select which bits of the operands participate in the logical operation, comprising the steps of:

a. Allowing a partial instruction to be executing during the instruction dispatch cycle of the computer system by providing said integer execution unit (FXU) with a predetermination cycle pipeline stage created to accommodate a timing critical function used for execution of an instruction, and overlapping said predetermination cycle pipeline stage (E-1 stage) with a dispatch cycle of the Instruction Decode and Dispatch Unit (I-Unit) of said integer execution unit

(FXU) of a central processor (CP) of the computer system (see Col.12 lines 18-49).

28. Here, stage s1 of the PC (performance critical) pipeline, which is the predetermination stage (see Col.12 lines 18-20), overlaps with stage s2 of the NPC (non-performance critical) pipeline, which is a dispatch stage (see Col.12 lines 22-26). Because since there is no s2 stage in the PC pipeline (see Col.12 lines 22-26), the s1 stage of the PC pipeline performs the same dispatching function as stages s1 and s2 combined of the NPC pipeline (see Col.12 lines 18-27). Therefore, because the two pipelines operate in parallel (see Fig.4), instructions executed in stage s1 of the PC pipeline will inherently overlap those instructions executed in stage s2 in the NPC pipeline. Also, because logical instructions such as AND, OR and XOR can use immediate operands (see Col.1 lines 40-53 and Col.1 line 66 – Col.2 line 4), they inherently contain the ability to use the operand as a mask, effectively selecting which bits are involved in the execution of the function. Furthermore, because full instructions are executing in each pipeline during the dispatch stages, inherently a partial instruction is executing during the dispatch stages also.

29. Regarding claim 2, Leung has taught the method according to claim 1, wherein the process proceeds by dividing a timing critical function used for execution of an instruction into first and second partitioned processes partitioned among a first and a second pipeline stage of a single pipeline. Here, instructions that are deemed performance critical are executed in the PC pipeline (see Col.11 lines 17-30, 53-61), and are executed in standard pipeline fashion, with multiple stages of execution for each performance critical instruction (see Col.1 lines 15-29), and are thus inherently divided into separate steps that execute in multiple stages of a single pipeline.

30. Regarding claim 3, Leung has taught the method according to claim 2, wherein said first partitioned process has said predetermination cycle (em1) which initiates two cycles before a first cycle of execution of said instruction when the input operands feed the ALU and the result is put into a result register and which initiates the timing critical function for execution of an instruction to be executed (see Col.12 lines 18-31). Here, the stage s3 is the register file write stage, writing the result of the ALU operation to the working register file (see Col.6 line 59 – Col.7 line 7). Because each stage occurs in one clock cycle, and the predetermination cycle is considered stage s1 (see above paragraph 28), there is two cycles between the initiation of stage s1 and the execution in stage s3.

31. Regarding claim 4, Leung has taught the method according to claim 3, wherein the second partitioned process, which includes said dispatch cycle (stage s2 of NPC pipeline), has a first cycle (e0) (stage s1 of NPC pipeline) and a second cycle (e1) (stage s3 of NPC pipeline) and a third cycle (PA) (stage s9 of NPC pipeline) (see Col.12 lines 18-31).

32. Regarding claim 5, Leung has taught the method according to claim 4, wherein:

a. Said first cycle (e0) is initiated when an instruction is being decoded to determine what instruction it is in order to setup the controls to the computer system ALU and the second partitioned process is used for reading and loading operands into a plurality of FXU input registers of said computer system's FXU which cycle determines whether the timing critical function of said predetermined cycle is valid for an instruction to be executed (see Col.7 lines 8-24 and Col.12 lines 18-20), and the second cycle (e1) performs the first cycle of execution of said instruction where the input operands feed the ALU and the result is put into a

result register (see Col.12 lines 23-31). Here, the stage s1 of the NPC pipeline performs the decoding of the instructions, as well as loading the source operands into input registers (see Col.7 lines 8-24). Furthermore, the stage s3 of the NPC pipeline performs the arithmetic execution on the operands, writing the results into registers (see Col.6 line 59 – Col.7 line 7 and Col.12 lines 23-31).

b. Wherein during the third cycle (PA) the contents of the result register are sent to an architected General Purpose Register file (GPR) (see Col.6 lines 59-63 and Col.12 lines 18-21).

33. Regarding claim 6, Leung has taught the method according to claim 5, wherein said third cycle is a dispatch cycle (stage s2 of NPC pipeline) (see Col.12 lines 18-31 and above paragraph 18).

34. Regarding claim 7, Leung has taught the method according to claim 5, wherein said timing critical function is a mask generation process (see Col.11 lines 44-61). Here, because logical instructions such as AND, OR and XOR can use immediate operands (see Col.1 lines 40-53 and Col.1 line 66 – Col.2 line 4), they inherently contain the ability to use the operand as a mask, effectively selecting which bits are involved in the execution of the function.

35. Regarding claim 8, Leung has taught the method according to claim 5, wherein said timing critical function determines read addresses for the GPR's of said computer system (see Col. 11 lines 31-61). Here, timing critical instructions that execute in the performance critical pipeline determine read and write addresses to write back to the working register file, which corresponds to the architectural register file (see Col.7 lines 24-32 and Col.7 line 55 – Col.8 line 16).

36. Regarding claim 9, Leung has taught the method according to claim 5, wherein in the process allowing a partial instruction to be executing during the instruction dispatch cycle of the computer system, the three pipeline cycles of the second partitioned process said pipeline stages work independently so that they contain three different instructions in various states of execution (see Col.1 lines 15-29). Here, it is inherent in the operation of a pipeline with a plurality of stages (s1-s9) that instructions in different states of execution are in the pipeline simultaneously at all times.

37. Regarding claim 10, Leung has taught the method according to claim 5, wherein the first partitioned process overlaps with the I-unit instruction pipeline as well as with the execution cycles of earlier in the pipeline instructions (see Col.12 lines 18-49). Here, stage s1 of the PC (performance critical) pipeline, which is the predetermination stage (see Col.12 lines 18-20), overlaps with stage s2 of the NPC (non-performance critical) pipeline, which is a dispatch stage (see Col.12 lines 22-26). Because since there is no s2 stage in the PC pipeline (see Col.12 lines 22-26), the s1 stage of the PC pipeline performs the same dispatching function as stages s1 and s2 combined of the NPC pipeline (see Col.12 lines 18-27). Therefore, because the two pipelines operate in parallel (see Fig.4), instructions executed in stage s1 of the PC pipeline will inherently overlap those instructions executed in stage s2 in the NPC pipeline.

38. Regarding claim 11, Leung has taught the method according to claim 5, wherein said predetermination cycle pipeline stage is used to accommodate a first part of the mask generate process, and this predetermination cycle pipeline stage (E-1 stage) is inserted before a pipeline execution stage (E0 stage). Here, because logical instructions such as AND, OR and XOR can use immediate operands (see Col.1 lines 40-53 and Col.1 line 66 – Col.2 line 4), they inherently

contain the ability to use the operand as a mask, effectively selecting which bits are involved in the execution of the function. Furthermore, because the first stage in the execution of any instruction, let alone a logical instruction, is the predetermination stage s1 of the PC pipeline, it is inherently before stage s2, the execution stage (see Col.6 line 64 – Col.7 line 7), and is therefore beginning the execution of an instruction using a mask from an immediate operand.

39. Regarding claim 12, Leung has taught the method according to claim 11, wherein said predetermination cycle pipeline stage (stage s1 of the PC pipeline) does not increase the depth of the FXU pipeline and overlaps with the last stage or dispatch stage of the Instruction Decode and Dispatch Unit (I-Unit) (stage s2 of the NPC pipeline). Here, stage s1 of the PC (performance critical) pipeline, which is the predetermination stage (see Col.12 lines 18-20), overlaps with stage s2 of the NPC (non-performance critical) pipeline, which is a dispatch stage (see Col.12 lines 22-26). Because since there is no s2 stage in the PC pipeline (see Col.12 lines 22-26), the s1 stage of the PC pipeline performs the same dispatching function as stages s1 and s2 combined of the NPC pipeline (see Col.12 lines 18-27). Therefore, because the two pipelines operate in parallel (see Fig.4), instructions executed in stage s1 of the PC pipeline will inherently overlap those instructions executed in stage s2 in the NPC pipeline. Furthermore, because the s1 stage of the PC pipeline already exists, it is inherently not increasing the depth of the FXU pipeline.

40. Regarding claim 13, Leung has taught the method according to claim 1, wherein said predetermination cycle pipeline stage (stage s1 of PC pipeline) also provides cycle time relief of the execution (e0) stage (stage s2 of PC pipeline) by allowing an extra cycle to decode the instruction and form GPR read addresses which need to be launched directly from latches at the beginning of the E0 cycle (see Col.12 lines 18-20). Here, because in the PC pipeline where the

predetermination stage exists every stage takes one clock cycle to execute (see Col.11 lines 30-43), there is one cycle to decode the instruction and form GPR read addresses between the s1 stage and the s2 stage (see Col.6 line 64 – Col.7 line 24).

41. Regarding claim 14, Leung has taught the method according to claim 1, wherein said predetermination cycle pipeline stage is a stage of the mask generator logic which overlaps with the I-unit instruction unit as well as with the execution cycles of older (earlier in the pipeline) instructions. Here, because logical instructions such as AND, OR and XOR can use immediate operands (see Col.1 lines 40-53 and Col.1 line 66 – Col.2 line 4), they inherently contain the ability to use the operand as a mask, effectively selecting which bits are involved in the execution of the function. Furthermore, stage s1 of the PC (performance critical) pipeline, which is the predetermination stage (see Col.12 lines 18-20), overlaps with stage s2 of the NPC (non-performance critical) pipeline, which is a dispatch stage (see Col.12 lines 22-26). Because since there is no s2 stage in the PC pipeline (see Col.12 lines 22-26), the s1 stage of the PC pipeline performs the same dispatching function as stages s1 and s2 combined of the NPC pipeline (see Col.12 lines 18-27). Therefore, because the two pipelines operate in parallel (see Fig.4), instructions executed in stage s1 of the PC pipeline will inherently overlap those instructions executed in stage s2 in the NPC pipeline.

42. Regarding claim 15, Leung has taught the method according to claim 1, wherein said predetermined cycle pipeline stage is implemented as a speculated pipeline stage in which the validity of said predetermined cycle pipeline stage is not known until a following execution stage, wherein if an execution (E0) stage first becomes valid, it is implied that the predetermined

cycle pipeline (E-1) stage was valid on the cycle before, without impacting a subsequent dispatch stage of said I-Unit (see Col.7 lines 45-54).

43. Regarding claim 16, Leung has taught the method according to claim 1, wherein said predetermined cycle pipeline stage of an instruction overlaps with the execution stages of previous instructions (see Col.1 lines 15-29). Here, the pipelines operate as conventional pipelines, which inherently have stages of new instructions overlapping with stages of older instructions.

Conclusion

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

45. Narayan, U.S. Patent No. 5,935,239, has taught a method for mask generation in parallel with the execution of the instruction it will be used upon.

46. Davies, U.S. Patent No. 5,651,121, has taught a method of obtaining a mask operand from an immediate operand within an instruction.

47. Jones et al., U.S. Patent No. 4,750,112, has taught a processor with an instruction pipeline and an execution pipeline which overlap for certain stages.

48. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

49. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
2/23/2004

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